

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Nishant Sinha

**Serial No.:** 10/668,914

**Filed:** September 23, 2003

**For:** PROCESS AND INTEGRATION  
SCHEME FOR FABRICATING  
CONDUCTIVE COMPONENTS,  
THROUGH-VIAS AND  
SEMICONDUCTOR COMPONENTS  
INCLUDING CONDUCTIVE THROUGH-  
WAFER VIAS

**Confirmation No.:** 2525

**Examiner:** W. Lindsay Jr.

**Group Art Unit:** 2812

**Attorney Docket No.:** 2269-5859US  
(02-0390.00/US)

**VIA ELECTRONIC FILING**  
**June 25, 2007**

**FEE ADDRESSEE FOR RECEIPT OF PTO NOTICES  
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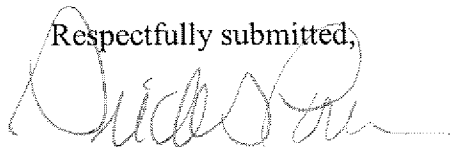
Sir:

1. This letter is to specify that the FEE ADDRESSEE for this patent is:

MICRON TECHNOLOGY, INC.  
Mail Stop 525  
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2. The Customer Number for the Fee Addressee is **26809**.
3. Any prior FEE ADDRESSEE for this patent is hereby revoked.
4. It is certified that the person whose signature appears below has the authority to change the FEE ADDRESSEE for this patent.

Respectfully submitted,



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BGP/dlm:eg  
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